ABSTRACT OF THE DISCLOSURE

In a multiprocessor system of a hierarchy configuration as a parallel computer of a common-bus structure, a processing unit (120) in an intermediate stage has a processor (123) having a programmable function that is equal to a normal processor, an instruction memory (125), and a data memory (127). The processing unit (120) receives a status signal from a lower processor (143), and a DMA controller (151) having a memory for the transfer of large sized data performs compression, decompression, programmable load dispersion, and load dispersion according to the state of operation of each lower processor.